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10EC45

Fourth Semester B.E. Degree Examination, Dec.2017/Jan.2018
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. List different types of description in HDL. Explain structural and behavioral description with example. **(10 Marks)**

b. Given unsigned variables A, B, C with A = 11001011 B = 10110110, C = 00011011 find the value of
i) A ror 1 ii) A NAND C iii) B Sra 1 iv) ~ 1 C **(04 Marks)**

c. Explain scalar data types with syntax. **(06 Marks)**

2 a. Write a Verilog code for 2×2 unsigned combinational array multiplier with diagram. **(08 Marks)**

b. Write a VHDL code in data flow description for two bit magnitude comparator with simplified boolean expression. **(12 Marks)**

3 a. Write a VHDL code for D – Latch using signal and variable assignment statement. With simulation waveforms clearly distinguish between them. **(10 Marks)**

b. Explain for loop, while loop, Next and Exit in VHDL. **(04 Marks)**

c. Write a verilog code for 2×1 multiplexer with tristate output using IF-else statement. **(06 Marks)**

4 a. Write a structural description in VHDL for full adder with simulation waveform. **(08 Marks)**

b. Explain binding between :
i) Entity and Architecture
ii) Entity and component
iii) Library and module. **(06 Marks)**

c. Write a Verilog code for N-bit asynchronous down counter using generate statement. **(06 Marks)**

PART – B

5 a. Write a VHDL code to perform signed vector multiplication using procedure. **(10 Marks)**

b. Write a Verilog function to find greater of two signed number. **(05 Marks)**

c. Write a note on Verilog file processing. **(05 Marks)**

6 a. Explain the implementation of single and two dimensional arrays in VHDL. **(04 Marks)**

b. Write a VHDL code for addition of two 3×3 matrices. **(06 Marks)**

c. With a block diagram and function table write a VHDL code for 16×8 SRAM. **(10 Marks)**

7 a. Explain how to invoke Verilog module from a VHDL module. **(08 Marks)**

b. Write mixed language description of a 3-bit adder with zero flag. **(12 Marks)**

8 a. Describe the synthesis information extraction from entity and module with examples. **(10 Marks)**

b. With an example; explain synthesis of loop statement and show RTL synthesis. **(10 Marks)**

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